

4W, W-band GaN Solid-State Power Amplifier

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Abstract: This paper describes a W-band solid-state power amplifier which produces an output power of greater than 4 watts from 94 to 98 GHz and a peak power of 5 watts at 98 GHz. These state-of-art (SOA) results were achieved by combining four SOA 1W GaN MMICs in a low-loss waveguide power combining network.

Keywords: MMIC; Power Amplifier; Septum Combiner; W-band; GaN; millimeter-wave; SSPA

Introduction

Current and future military systems require transmitter output power levels ranging from several watts to perhaps 50 watts or more at W-band frequencies (75-110 GHz). Solid-state power amplifiers (SSPAs) are preferred over tube amplifiers due to their high reliability, low cost and broad-bandwidth capability. Using conventional GaAs and InP MMIC technologies, output power levels are currently limited to several hundred milliwatts [1]. Recent advances in wide bandgap GaN technology have enabled the realization of millimeter-wave MMICs producing multi-watt power levels [2-4]. To achieve still higher power levels, power combining techniques must be employed. Previously, 12-way radial and 4-way septum power combiners were used to achieve power levels up to 5 watts at 95 GHz [5-7]. Utilizing the latest GaN MMIC technology, this paper presents the design and performance of a new 4-way amplifier/combiner that produces an output power of greater than 4 watts from 94 to 98 GHz and a peak output power of 5 watts at 98 GHz. This work establishes new performance benchmarks for solid-state power amplifiers operating at W-band frequencies.

W-band GaN Process and MMIC Design

The MMICs used in this work were designed by QuinStar and fabricated by HRL Laboratories using their 1st generation GaN process. With a gate length of typically 0.14 μm , this process produces GaN devices with typical f_T and f_{max} values of 90 and 200 GHz, respectively. Although the 2nd generation GaN process is purported to provide a higher output power and PAE [2], at the time of the MMIC development, the 2nd generation process was not available.

The GaN MMIC, with chip dimensions of 3.8 x 2.1 mm², is shown in Figure 1. This is a 3-stage, balanced amplifier configuration with Lange couplers and microstrip matching elements. The gate periphery ratios for the 3 stages are 1:2:4 with a unit cell size of 150 μm . The resulting total output gate periphery is 1200 μm .

The on-wafer, small-signal characteristics of this MMIC are shown in Figure 2. The small-signal gain is typically 12 dB from 90 to 98 GHz with an excellent input/output match. Due to the balanced structure, the input/output return loss is typically 15 dB or better.

The output power characteristics are summarized in Figure 3. In this figure the MMIC output power is plotted versus frequency for different drive levels. The data has been corrected for the fixture loss. At an input drive of 22 dBm, the MMIC achieves an output power of greater than 30.5 dBm (1.12 W) from 94 to 100 GHz with a maximum of 31.6 dBm (1.44 W) at 98 GHz. While higher power levels have been reported at W-band with narrow-band MMICs, these results represent the highest broadband GaN MMIC results reported to date.

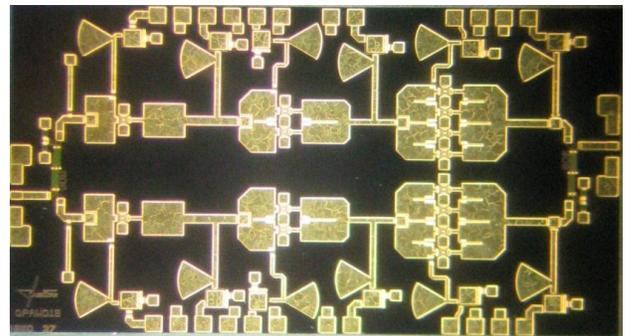


Figure 1. W-band MMIC fabricated using HRL's GaN process. Chip dimensions are 3.8 x 2.1 mm².

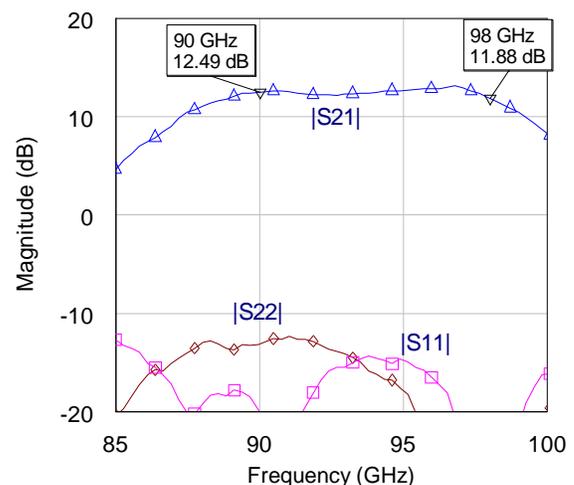


Figure 2. On-wafer small-signal MMIC data. The chip is biased at $V_{ds} = 12\text{V}$.

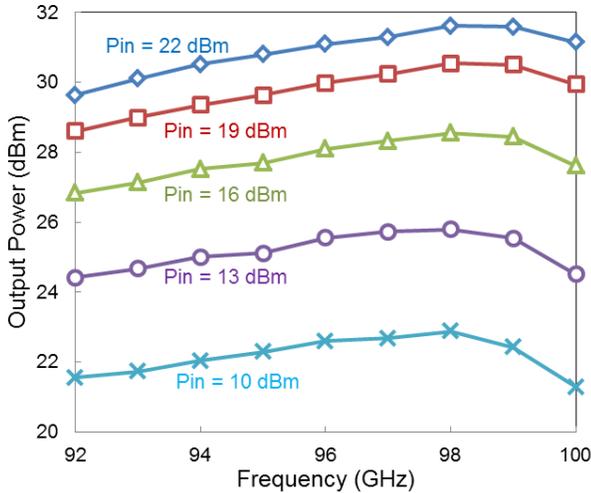


Figure 3. Measured output power of the MMIC with different input power levels. The MMIC is biased at $V_{ds} = 14V$.

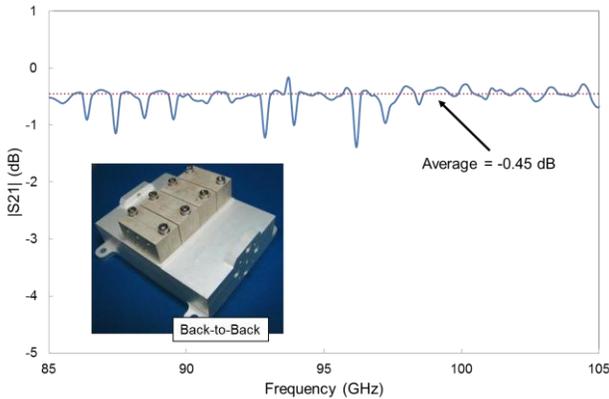


Figure 4. Back-to-back measurement of the 4-way septum combiner indicates a loss of less than 0.25 dB per combiner.

Septum Combiner and Unit Amplifier

To achieve higher power levels, we combined four of these MMICs using a high-efficiency septum combiner approach. This approach has previously demonstrated combining efficiencies of 93% at W-band [4,5]. For this work, we used a similar combiner structure with a different input/output feed. This new arrangement allows the input and output ports to be in-line and the unit amplifiers to be mounted next to each other for a more compact configuration. The resulting overall size of the combiner housing is 2.5 x 2.43 x 0.75 inches. The back-to-back “cold” test (Figure 4) revealed an average loss of less than 0.5 dB. This implies a combiner loss of less than 0.25 dB and a potential combining efficiency of 94%.

The MMIC was mounted on a chip carrier that includes waveguide-to-microstrip transitions and bypass capacitors. We call this assembly, shown in Figure 5, a “unit amplifier” (UA). Several UAs were characterized for power, and the four best UAs were selected to be used in

the combiner. Table 1 summarizes the performance of the four selected UAs.

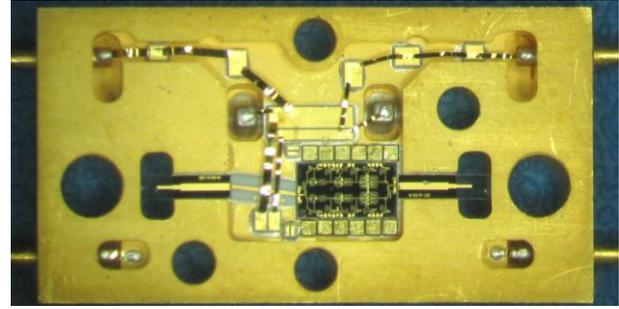


Figure 5. The unit amplifier consists of the MMIC chip with associated bias and decoupling capacitors and waveguide-to-microstrip transitions.

Table 1. Unit amplifiers’ performance at 98 GHz

S/N	Pout (dBm)	Id (A)	PAE (%)
4950	31.21	0.757	10.57
5050	31.03	0.747	9.09
5149	31.3	0.777	9.49
5150	31.13	0.768	9.12
Total	37.18	3.049	9.302

The UAs were tested at a drain bias of 14V and at an input power level of 25 dBm. The table summarizes the performance at 98 GHz, where peak power and PAE occur. The four selected UAs produce output power levels that are matched to within 0.3 dB of each other.

The last row in the table indicates the algebraic sum of the four UA’s output power, 37.18 dBm or 5.22W. This represents the output power level we could expect with a perfect (lossless) combiner. However, due to the finite loss of the combiner network, and further, due to power and phase imbalances between the UAs, we expect a lower output power level. Based on dissipation losses alone (0.25 dB), the best this combiner can produce is 4.93W (94% of the total).

Amplifier/Combiner Performance

The four selected UAs were mounted on the combiner housing as shown in Figure 6. The PCBs shown in the figure provided the necessary bias voltages for each UA. The small-signal performance of the amplifier/combiner is shown in Figure 7. It reveals a gain of typically 12 dB from 90 to 98 GHz, identical to the gain response of each UA.

The test system used to evaluate the power performance the amplifier/combiner is shown in Figure 8. As shown we used one of the extra UAs to drive this amplifier/combiner. The measured results are plotted in Figures 9 and 10. The results include both the driver and the amplifier/combiner. For all of these tests, the amplifier was operating under CW conditions.

Figure 9 shows the output power as a function of frequency for different input drive levels, and Figure 10 illustrates the power compression characteristics at 98 GHz. As shown in Figure 9, the amplifier/combiner produces an output power of greater than 36 dBm or 4 watts from 94 to 98 GHz.

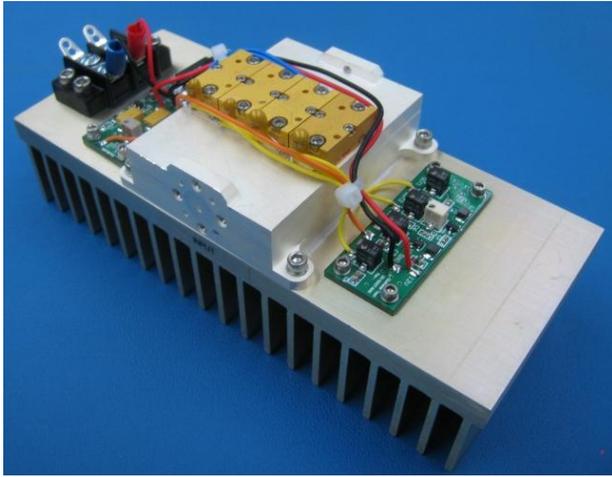


Figure 6. W-band SSPA with UAs mounted on the 4-way septum combiner housing.

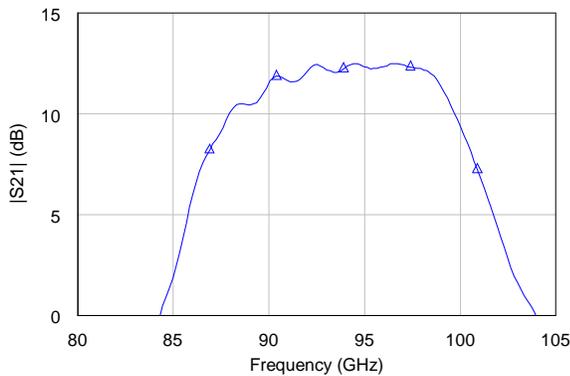


Figure 7. Small signal performance of the SSPA. It exhibits a gain of 12 dB across 90 to 98 GHz.

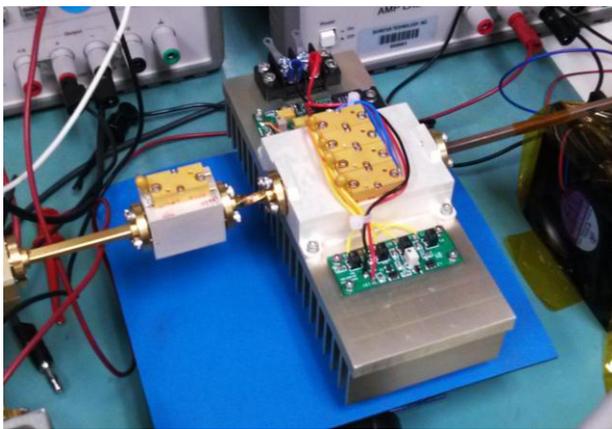


Figure 8. Power measurement test setup. A spare unit amplifier is used as a driver to drive the SSPA.

When biased at 15 V, the amplifier achieves a peak output power of 37 dBm or 5 watts at 98 GHz. The output power of the amplifier is ultimately limited by the power provided by the driver.

By comparing the output power level of this amplifier/combiner to the UA sum in Table 1, we can estimate the combining efficiency. Under the same drive and bias conditions, this amplifier produced an output power of 36.9 dBm or 4.85W at 98 GHz. This represents a combining efficiency of about 93%, and is very close to the theoretical efficiency due to conductor losses only. This seems to imply that the unit amplifiers are well matched.

The overall PAE of this amplifier/combiner is only 9%, which is due primarily to the GaN MMIC chips. The PAE of the unit amplifiers is typically 9-10% as shown in Table 1.

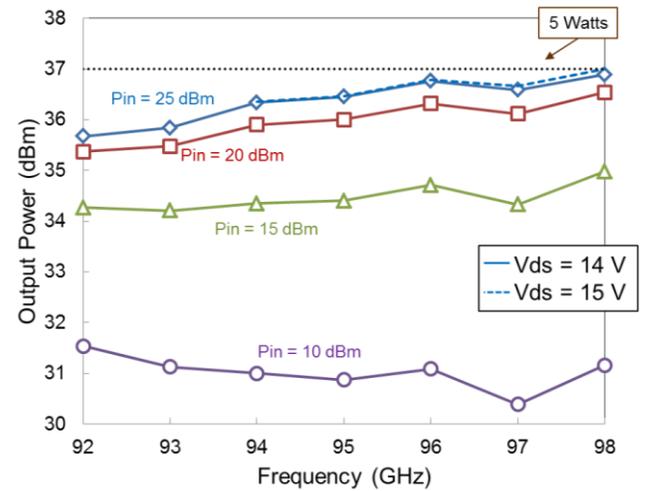


Figure 9. Output power response of the amplifier/combiner with input power as a parameter. A peak output power of 37 dBm or 5 watts was achieved at 98 GHz. $V_{ds} = 15$ V.

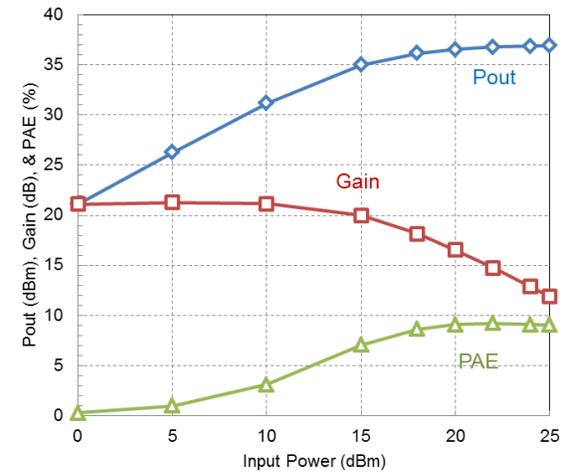


Figure 10. Power transfer characteristics of the SSPA and driver at 98 GHz. $V_{ds} = 14$ V.

Conclusion

In summary, this work produced new levels of performance for solid-state power amplifiers operating at W-band. We designed and fabricated a new GaN MMIC chip which produced SOA output power levels from 93 to 100 GHz. Using a septum combiner, we combined 4 of these MMIC chips to achieve an output power of greater than 4 watts over the 94 to 98 GHz band. Our work has demonstrated that GaN MMICs are now capable of producing multi-watt power levels at W-band frequencies, and by using high-efficiency combining techniques, power levels of tens of watts are now within reach.

Acknowledgements

This work was supported by the Naval Air Warfare Center under SBIR Contract N68335-10-C-0049.

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