F-Band, GaN Power Amplifiers

Edmar Camargo, James Schellenberg, Lani Bui, and Nicholas Estella
QuinStar Technology, Inc. Torrance, CA, 90505, USA

***Abstract*—This paper reports the design and performance of two new GaN MMIC amplifiers operating at F-band frequencies. The first design produces 28-29 dBm from 102 to 118 GHz, while the second, a broadband design, produces a minimum of 25 dBm across the 98 to 122 GHz band. Both designs exhibit a small-signal gain of 20 dB. In addition, we report a multi-MMIC SSPA with an output power of 2-3 W from 102 to 116 GHz. These are the first reported GaN power results above 100 GHz and the highest power level for any solid-state technology at this frequency.**

***Index Terms*— GaN MMIC, power amplifier, millimeter-wave, broadband amplifier, F-band.**

I. Introduction

Currently there is a need for solid-state power amplifiers (SSPAs), operating at 105-115 GHz, in support of NASA Earth Science missions. These SSPAs, with power levels of 1-4 W, are required to drive LO multiplier chains in Terahertz receivers. As the demand for higher data rates (bandwidth) increases, future military and 5G communications systems are also expected to benefit from this F-band SSPA technology.

Recent GaN MMIC work at E and W-band frequencies has produced MMICs with power levels of several watts [1-4], and utilizing power combining techniques, SSPAs with output power levels of 40 W are emerging [5]. Despite rapid progress at E and W-band, there is little published work on solid-state power above 100 GHz. There are, however, three notable exceptions: Teledyne has reported 85 mW at 118 GHz [6] and 250 mW at 180 GHz [7] using InP HBT technology, Northrop Grumman has reported 75 mW at 210 GHz [8], and JPL has demonstrated a 25 mW wideband MMIC covering the 105 to 140 GHz band [9]. In all three cases, InP technology was employed. To the author's knowledge, no one has reported GaN results above 100 GHz.

This paper presents GaN MMICs operating at frequencies of up to 122 GHz with output power levels of up to 29 dBm (0.8 W).

II. Unit Cell and Amplifier Architecture

The MMICs reported in this paper were fabricated by HRL Laboratories, Malibu, CA using their T2 GaN process (0.14 µm gate on 50 µm thick SiC) [10]. This process produces a double-heterostructure field-effect transistor (DHFET) with a typical I_{MAX} of 1 A/mm and f_T and f_{MAX} of 85 and 220 GHz, respectively.

For this work, we used a four-finger unit cell with 25 µm long gate fingers for a total unit cell gate periphery of 100 µm. The unit cell contains two vias and one internal non-viaed source island. The small-signal equivalent circuit of the unit cell is shown in Fig 1, and its performance in a pre-matched test circuit is shown in Fig. 2. The layout of the test circuit is also shown in the figure. It was tested over the 70 kHz to 145 GHz band, and the data indicates a maximum gain of 8.44 dB at 87 GHz. Based on a 6-dB per octave roll-off, this is equivalent to a f_{MAX} of 230 GHz. Operating at 12 V, the unit cell delivers a power density of typically 1.8 W/mm and a maximum PAE of 28-30% at 87 GHz.

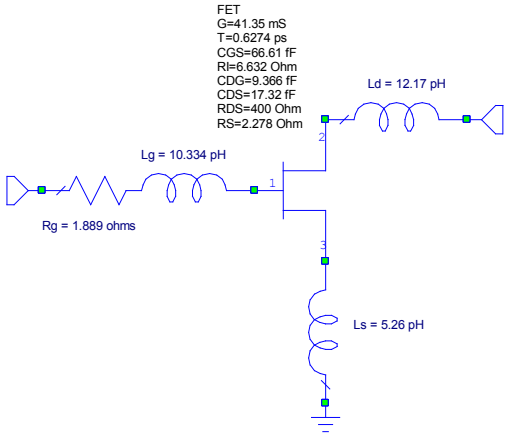


Fig. 1. Small-signal equivalent circuit model for the 4x25 µm unit cell. Bias: 12 V and Ids = 30 mA.

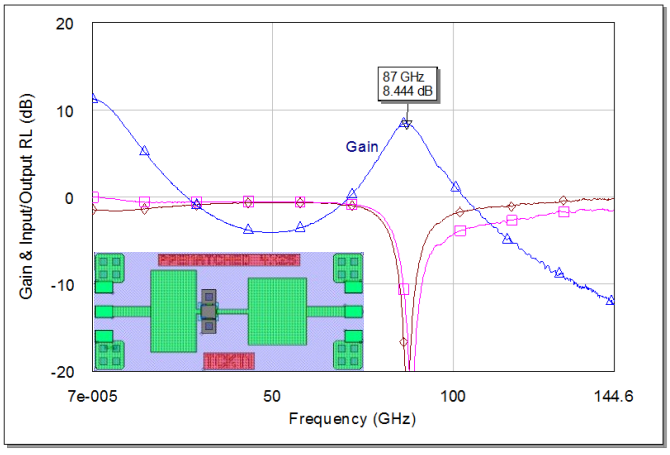


Fig. 2. Measured data of 4x25 µm unit cell in a pre-matched test circuit (insert) biased at 12 V and 27 mA (27% of I_{MAX}).

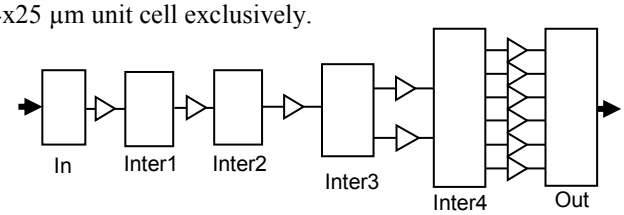
We designed two different amplifiers: one targeting broadband driver applications (called D1) and another for power (called D2). The design specifications are summarized below in Table 1. Due to circuit losses and the low device gain (5.5

dB MAG at 120 GHz), we need five gain stages to obtain an overall small-signal gain of 20 dB.

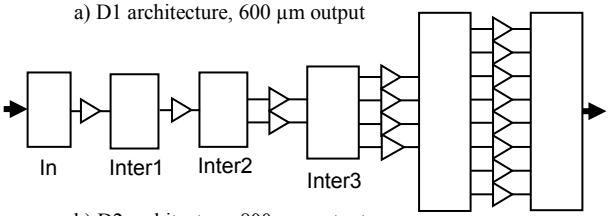
Table 1. Design specifications for the F-band MMICs

Parameter	Driver (D1)	Power (D2)
Pout (dBm)	26	29
Frequency (GHz)	100 - 120	105 - 115
SS gain (dB)	20	20

The block diagrams for the two MMICs are shown in Fig. 3. The output periphery for the broadband D1 design is 600 µm, while that of the D2 design is 800 µm. Both designs use the 4x25 µm unit cell exclusively.



a) D1 architecture, 600 µm output



b) D2 architecture, 800 µm output

Fig. 3. MMIC block diagrams, employing 4x25 µm unit cells.

III. MMIC Design and Layout

A. Power D2 Design

The D2 MMIC is shown in Fig. 4. Starting at the output, it uses an on-chip cell combining network to sum the power from the eight output cells and to simultaneously perform the impedance transformation between the cells and the external 50 Ω load. The simulated insertion loss of the combiner (above the ideal 8-way power division loss) is typically 0.7 dB and the amplitude balance between ports is ±0.5 dB. The phase balance between the ports is about ±5° over the band.

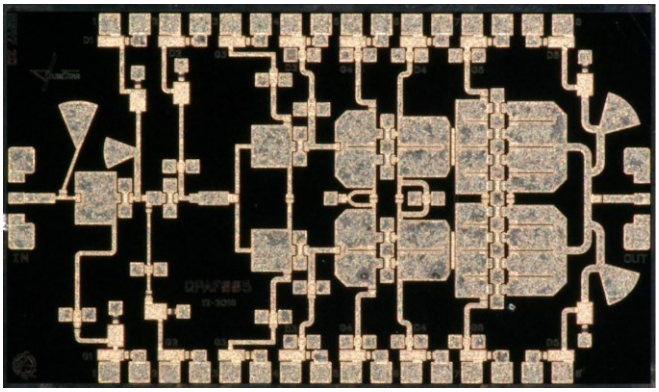


Fig. 4. D2 MMIC (chip size: 3.3 x 1.94 mm^2)

Quarter-wave transformers separated by a series capacitor Y-inverter are used for the interstage matching. The simulated gain for this amplifier indicates a 1-dB positive gain slope within the band, compensating for parasitics and device gain roll-off effects.

B. Broadband D1 Design

The D1 MMIC is shown in Fig. 5. It uses a 6-way cell combining network in the output stage network. This circuit is less complex than the 8-way combiner described above, and hence, we were able to achieve better magnitude and phase balance between the ports. The EM simulated amplitude and phase imbalance is ±0.3 dB and less than 2°.

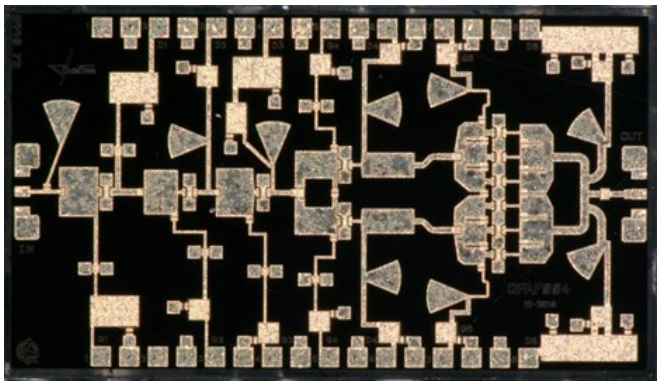


Fig. 5. D1 MMIC (chip size: 3.6 x 1.94 mm^2)

IV. Chip Measurements

A. Small-Signal Measurements

The MMICs were first characterized (70 kHz to 145 GHz) on-wafer using a Cascade Microtech probe station with 0.8 mm coax probes and an Anritsu ME7838D VNA. For this on-wafer work, the bias conditions were reduced to minimize self-heating effects.

The measured results for D2 compare favorably with simulations as shown in Fig. 6. The measured gain is nearly constant at 19.7 to 20.9 dB over the design band. Further, the data indicates that a resonance, originally simulated at 91 GHz, has moved up in frequency to about 98 GHz, but it is still out of the band of interest (105 to 115 GHz).

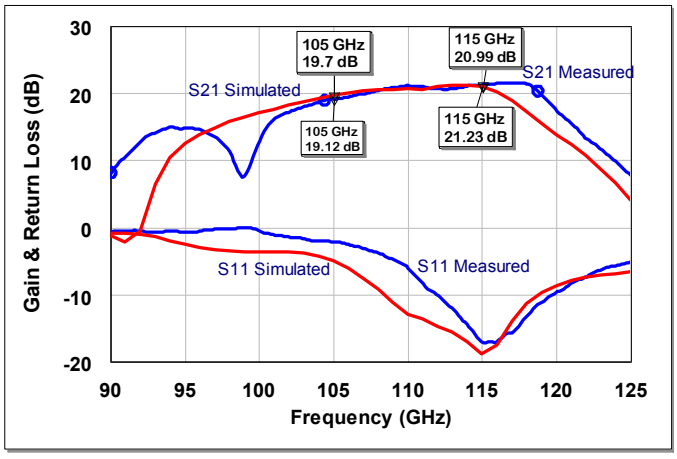


Fig. 6. Measured (blue) and simulated (red) small-signal performance of D2

The small-signal on-wafer measurements for D1 are presented in Fig. 7 together with simulations. The measured data is plotted in blue, while the simulated data is shown in red. The measured gain is greater than 20 dB from 92 to 123.5 GHz. The simulated gain is typically 2-3 dB lower and does not extend as high in frequency. We believe the differences are due to the device model.

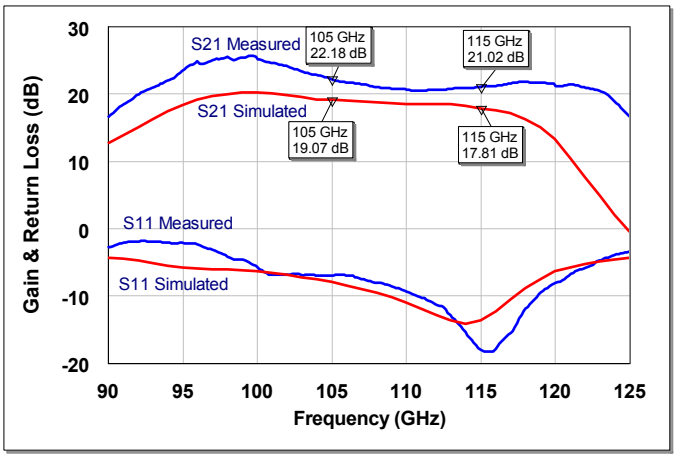


Fig. 7. Measured (blue) and simulated (red) small-signal performance of D1

B. Power Measurements

The MMICs were then diced and individually epoxied on a gold-plated copper carrier for power evaluation. The power performance of the D2 design is illustrated in Fig. 8. At 5 dB gain compression, the output power is flat at 28 to 29 dBm from 102 all the way to 118 GHz. The power between 118 to 120 GHz shows a sharp drop-off with frequency, which we believe is due to the 1-mm coax used in the wafer probe test system. The power-added efficiency of this MMIC is typically 8% over the 102 to 118 GHz band with a peak of 9.3% at 118 GHz.

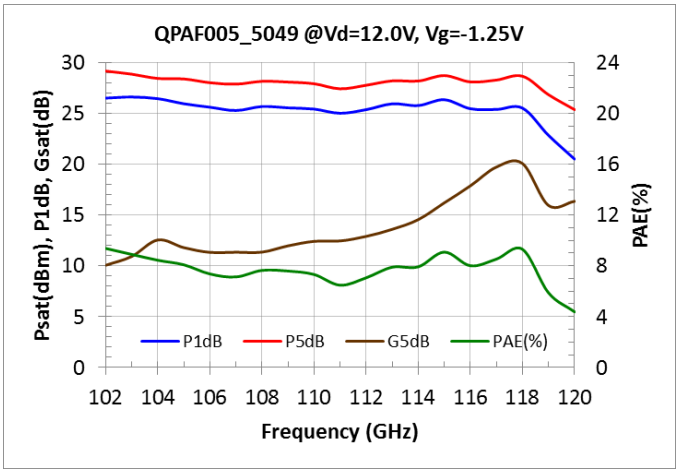


Fig. 8. D2 power performance at 5 dB compression.

The power results for D1 are plotted in Fig. 9. It produces an output power (P_{6dB}) ranging from 28 to 25 dBm over the 98-122 GHz band. While the PAE is only 6-7% across most of the upper part of the band, it rises to a peak of 14.4% at 102 GHz. The associated gain is 19 dB at the low end of the band, falling to 12 dB at midband before rising to 17 dB at the high end of the band.

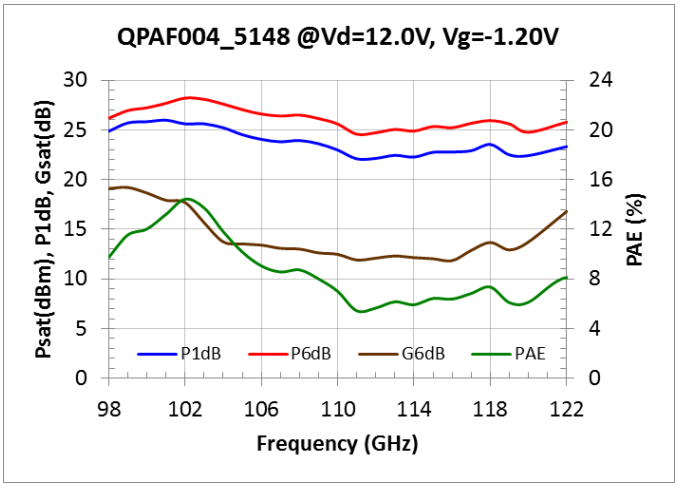


Fig. 9. D1 power performance at 6 dB compression.

The power performance for both MMICs, over the design band of 105 to 115 GHz, is summarized in Table 2. Over this bandwidth, D1 produces an output power (P_{6dB}) ranging from 24.6 to 27 dBm, while D2 yields a power level (P_{5dB}) of 27.6 to 28.9 dBm (0.78 W).

Table 2. MMIC performance over the 105-115 GHz band

MMIC	P_{1dB} (dBm)	P_{6dB} (dBm)
D1	22.1 - 24.5	24.6 - 27.0
D2	25.0 - 26.4	27.6 - 28.9

In addition to these chip-level measurements, we measured these MMICs at F-band frequencies in WR-8 waveguide test fixtures. D1 produced essentially the same result (minus the fixture losses), with an output power of 25 dBm extending to 124 GHz. D2's frequency response was more affected by the test fixture. It showed increased output power in the 102 to 116 GHz band and a peak of 29.6 dBm (0.91 W) at 112 GHz. The efficiency was also improved with a peak of 12.7% at 112 GHz.

Table 3. GaN MMIC Power at W and F-Band

Reference	CW Output Power	Frequency	PAE	Chip Size (mm^2)
[2] Brown	1.7 W at 91 GHz	90 – 92 GHz 2.2% BW	11% at 91 GHz	2.9 x 1.6
[3] Micovic	1.5 W	92 – 96 GHz 4.3% BW	20% at 93.5 GHz	NA
[11] Kim	1.2 W	94-100 GHz 6.2% BW	10% at 98 GHz	3.8 x 2.1
[4] Schellenberg	2.5 W ±1 dB	75-100 GHz 28.6% BW	12% at 84 GHz	5.4 x 2.75
[12] Margomenos	1.4 W	83 GHz	27%	NA
This work D1	24.6-27 dBm 0.5 W peak	98-122 GHz 21.8% BW	7% typ. 14% at 102	3.6 x 1.94
This work D2	28-29 dBm 0.9 W in fixture	102-118 GHz 14.5% BW	8% typ. 13% in fixture	3.3 x 1.94

To put this work in perspective, we summarize the GaN state-of-the-art above in Table 3. This table is limited to multi-stage MMIC amplifiers (no single-stage test circuits) operating above 75 GHz. While there are a number of results at W-band, nothing has been reported above 100 GHz other than this work.

V. F-BAND SSPA

Based on the MMICs described above, we designed, assembled and tested a 4-chip (using D2) combiner. This combiner was realized with binary H-tee WG junctions (2-tier). The size of this combiner module is 2.12 x 1.75 x 0.75 inch^3. The measured loss (at 120 GHz) of the back-to-back divider-combiner pair was 0.6 dB or 0.3 dB for each half. This includes the loss of the integrated WG-to-microstrip transition. We added an input driver module (again using D2) to boost the overall gain. The resulting SSPA configuration is shown in Fig. 10.

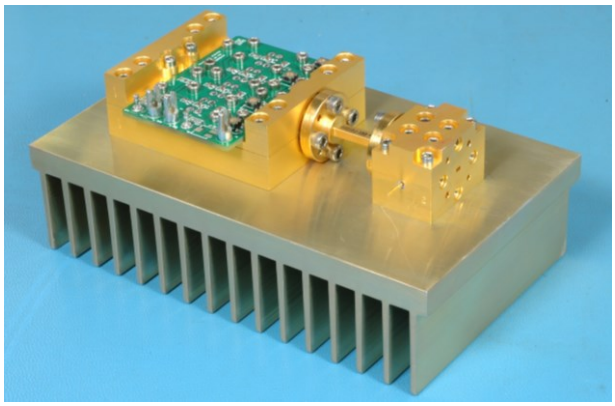


Fig. 10. Combiner and driver modules assembled on top of a heat sink

The performance of this SSPA, with an input drive level of 10 dBm, is summarized in Fig. 11. It produces an output power of greater than 2 W from 102 to 116 GHz with a peak of 2.75 W at 114 GHz. The associated gain is 23 dB or greater over this same band. The PAE is typically 6% with a peak of 7.8% at 114 GHz. This is the PAE for the entire SSPA including the driver module. The PAE for just the 4-chip combiner is typically 7.5% with a peak value of 9.4% at 114 GHz. The SSPA small-signal gain varies from 30 to 36 dB over this same band.

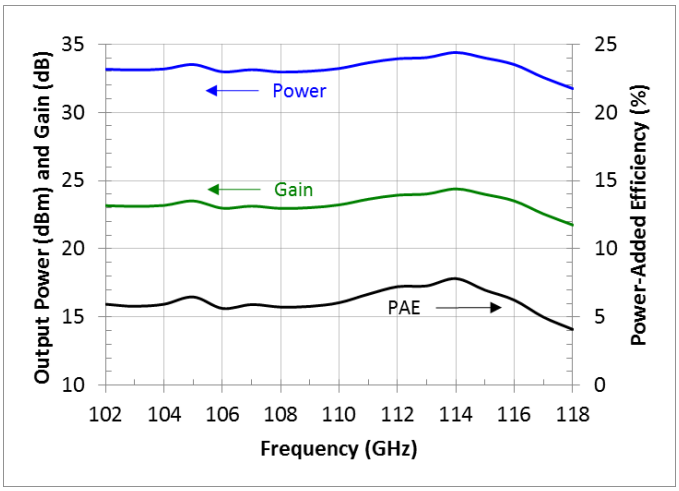


Fig. 11. Output power, gain and efficiency of the SSPA with a fixed input power of 10 dBm. Bias: 12V/-1.6V

VI. CONCLUSION

This work has established new power benchmarks for SSPAs operating at frequencies above 100 GHz. We have successfully demonstrated two GaN MMIC amplifiers operating at F-band frequencies: The first producing an output power of 28-29 dBm from 102 to 118 GHz, while the second, a wideband design, delivering an output power of greater than 25 dBm from 98 to 122 GHz. Lastly, we have assembled and tested a multi-MMIC SSPA producing an output power of 2-3 W over the 102 – 116 GHz band.

VII. ACKNOWLEDGMENT

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