High-Efficiency, Ka-band GaN Power Amplifiers

Nicholas Estella, Edmar Camargo, James Schellenberg and Lani Bui
QuinStar Technology, Inc. Torrance, CA USA

***Abstract*—This paper reports the design and performance of state-of-the-art GaN MMICs and a fully packaged Ka-band SSPA. Incorporating harmonic tuning, the MMICs produce power levels up to 10 W CW with efficiencies in the high thirties (42% peak) at frequencies of 30 to 34 GHz. These results represent the highest combination of CW power and efficiency at these frequencies. A 4-way combiner-SSPA, operating over 31 to 34 GHz, was assembled with these MMICs. Biased at 24 V, this SSPA produced an output power of greater than 20 W CW with an associated PAE of greater than 30% across the band. Biased for maximum power at 28 V, it achieved an output power of 32 W CW at 32.5 GHz with an associated PAE of 30%. This is the highest reported efficiency at this frequency for a packaged amplifier with greater than 30 W CW output power.**

***Keywords*— GaN MMIC, SSPA, power amplifier, Ka-band.**

I. Introduction

Current Ka-band applications, such as point-to-point communications, EW systems, satellite up and down links and 5G networks, are demanding improvements in power amplifier efficiency. Deep Space Network (DSN) applications are particularly sensitive to efficiency due to the limited available prime power. The required power levels generally range from tens of watts to perhaps several hundred watts with efficiencies of 30% or more. Using GaN technology, recent work has demonstrated remarkable advancements in both power and efficiency [1-14]. Single-chip MMICs with output power levels of up to 40 W pulsed have been demonstrated at 27 GHz with chip efficiencies of 36% [5]. However, no one has reported both high efficiency and high power in a single chip operating CW. The highest power level MMICs generally have poorer efficiencies or are operating in a short pulse mode.

This work presents the design and performance of two high efficiency harmonically tuned Ka-band MMICs. Operating from 29-31 GHz, the first MMIC (called D1) has demonstrated a peak PAE of 42% with an associated output power of 8 W. The second MMIC (called D2) has demonstrated power levels of 8-10 W over the 31-34 GHz band with a peak PAE of 36%.

To the authors' knowledge, this work represents the highest combination of CW power and efficiency at 30 GHz for a single GaN chip. Further, a packaged SSPA, using four D2 MMICs, has demonstrated the best combination of power and efficiency (32 W and 30% PAE) for a packaged amplifier operating over the 31-34 GHz band.

II. Unit Cell and Harmonic Terminations

The MMICs reported in this paper were fabricated by Northrop Grumman Aerospace Systems (NGAS) in Redondo Beach, CA using their GaN20 process (0.2 µm gate length on 100 µm thick SiC). This process yields a HEMT device with a typical I_{MAX} of 1 A/mm, a breakdown of 90 V and f_T and f_{MAX} of 40 and 100 GHz, respectively. The output power density is typically 4 W/mm for 24-28 V bias.

For the efficiency study, we used an 8x50 µm unit cell, which contains eight gate fingers, each 50 µm long. The internal source islands are air-bridged over to the via grounds on both sides. The small-signal equivalent circuit for this cell is shown in Fig 1. From the model, the f_T and f_{MAX} are 41 GHz and 114 GHz respectively.

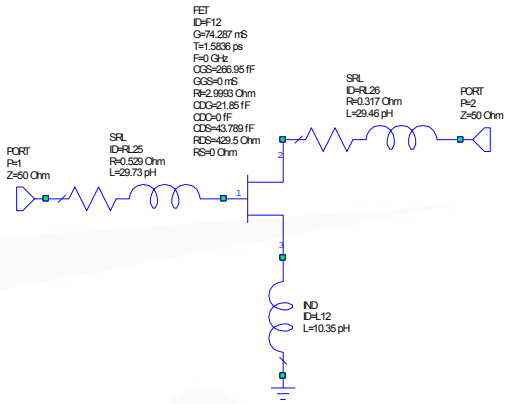

Fig. 1. Small-signal equivalent circuit model for the 8x50 µm unit cell. Bias: 28 V and Ids = 40 mA (100 mA/mm).

To investigate the cell matching conditions (fundamental and harmonic) for maximum efficiency, we performed a series of simulations using the foundry 8x50 µm non-linear model. The simulations revealed that on the drain side, the device was relatively insensitive to 2nd harmonic tuning, but it was sensitive to the phase (~180°) of the 3rd harmonic termination. On the gate side, the opposite was found to be true, with sensitivity to the 2nd harmonic termination and little sensitivity to the 3rd. These terminations are similar to what one would expect for inverse Class F operation.

To verify the model results, we fabricated and tested a series of test circuits (again using the 8x50 µm unit cell) with various combinations of fundamental and harmonic terminations. The test circuit yielding the best efficiency performance is shown in Fig. 2, together with its measured and simulated data. In addition to fundamental matching, this network presents a short circuit to the 2nd harmonic on the gate side, and a low impedance to the 3rd harmonic on the drain side. Biased near pinch-off (25 mA/mm) and 20 V, it produced a maximum PAE of 55% (63.3% drain efficiency) with an associated output power of 29.6 dBm (0.9 W). These results agree very well with simulation results (also shown) and indicate that harmonic tuning adds at least 5 percentage points to the efficiency.

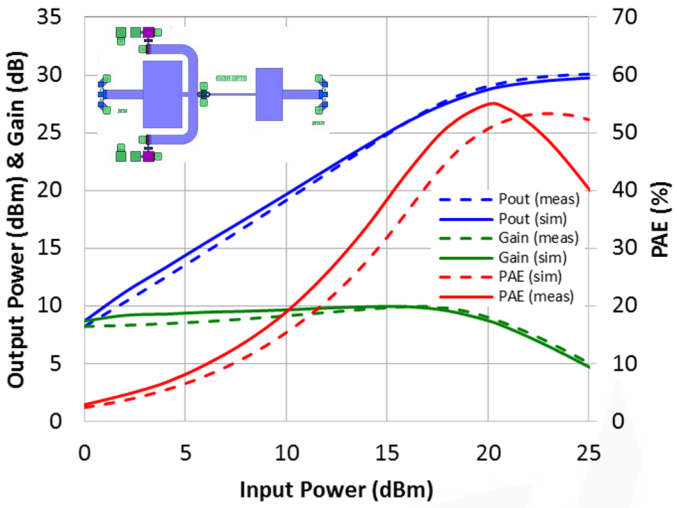

Fig. 2. Measured and simulated results at 30 GHz with pre-matched 8x50 µm unit cell. The test circuit is shown as an insert. Bias: 20 V and Idq=25 mA/mm.

III. MMIC Design and Layout

Based on the simulations and the empirical test cell work, we designed two different high-efficiency amplifiers: one (called D1) targeting narrowband 30 GHz applications and the second (D2) for the 31-34 GHz band. Both MMICs use a 3-stage topology and contain harmonic tuning to enhance efficiency. The device line-up for each MMIC is summarized in Table 1. The total output gate periphery for D1 and D2 is 2.4 and 1.84 mm respectively.

Table 1. Stage gate periphery for D1 and D2.

MMIC	Stage		
	1st	2nd	3rd
D1	4x30µm	2(8x50µm)	4(8x75µm)
D2	4x50µm	2(8x46µm)	4(8x57.5µm)

These two MMICs are shown in Figs. 3 and 4 respectively. With the exception of the harmonic tuning, the designs are conventional single-ended designs. For simplicity, we used harmonic tuning only in the final stage, with λ/4 shunt stubs providing short circuits to the gate at the 2nd harmonic and drain circuits designed to present a low impedance at the 3rd harmonic. There was no attempt to tune the 2nd harmonic in the output network.

IV. MMIC Measurements

A. Small-Signal Measurements

The MMICs were first characterized on-wafer using a Cascade Microtech probe station with an Anritsu ME7838D VNA. The small-signal D1 results (23 dB gain centered at 30 GHz) are unremarkable, and hence the plots are omitted. The D2 measurements and simulations are shown in Fig. 5. The measured gain is typically 27 dB over the 29 to 34 GHz band and compared to the simulation is shifted down in frequency by about 1.5 GHz.

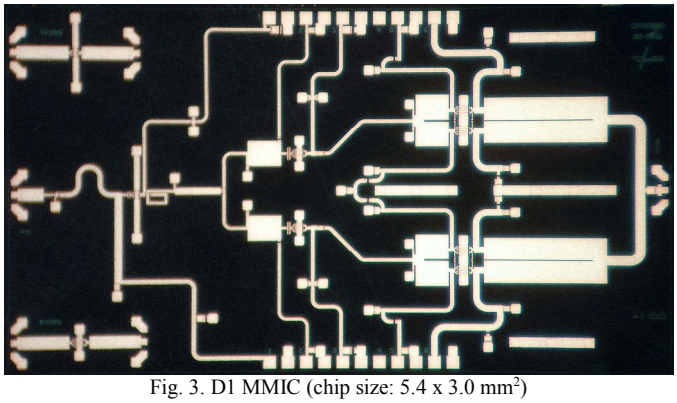

Fig. 3. D1 MMIC (chip size: 5.4 x 3.0 mm^2)

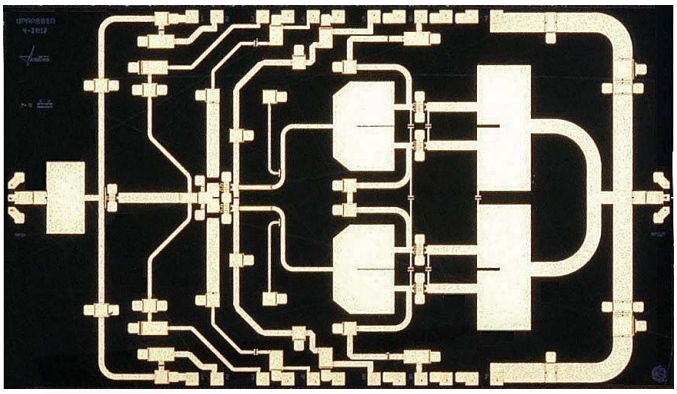

Fig. 4. D2 MMIC (chip size: 5.4 x 3.1 mm^2)

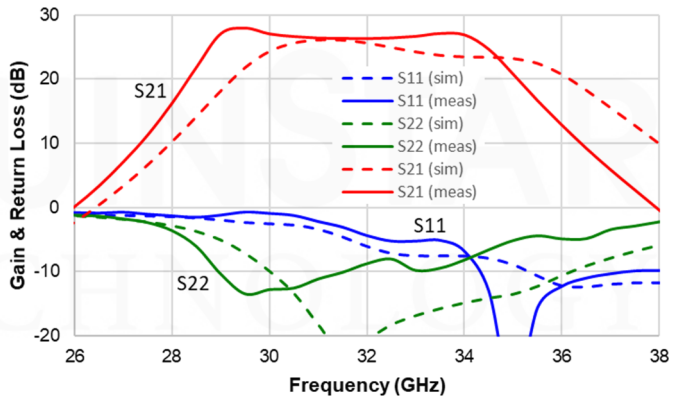

Fig. 5. On-wafer small-signal performance of D2 compared to simulations. Bias: Vd=28 V and Id=127 mA (45mA/mm).

B. Power Measurements

For power evaluation, the MMICs were mounted on a gold-plated copper carrier (serving as the heat sink) and RF probed. For comparison, some MMICs were assembled in Ka-band test fixtures. The results were similar. The power performance of D1 is illustrated in Fig. 6. At 3 dB gain compression, the average output power is 38.6 dBm (39.1 dBm peak) between 29 to 31 GHz. The PAE is greater than 38.6% over the 29.5 to 30.5 GHz band and peaks at 42% at 29.5 GHz. The power gain is better than 15 dB over this same band.

The typical power performance of D2 is plotted in Fig. 7, showing a power ranging from 39 to 40 dBm (10 W) over the

31 to 34 GHz band, with an associated gain of 24 to 25 dB. The PAE is greater than 30% across the band and reaches a peak of 36% at 33 GHz.

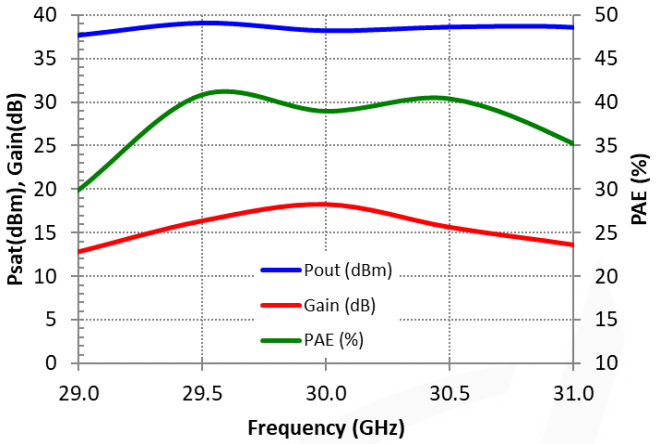

Fig. 6. D1 power and efficiency performance at P_{3dB}. Bias:28V

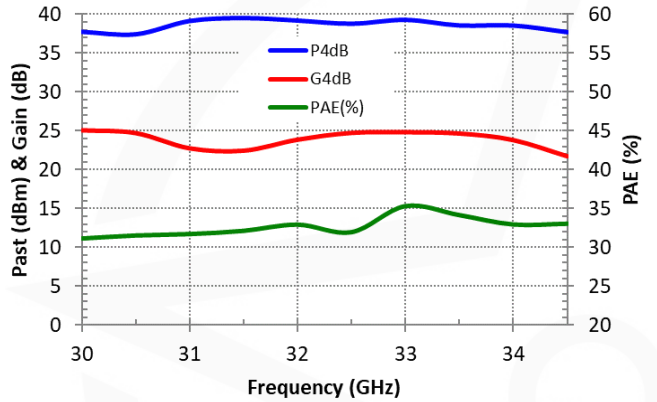

Fig. 7. D2 power and efficiency performance at P_{4dB} (P_{SAT}). Bias: 28V

To put this work in perspective, we summarize the GaN power state-of-the-art in Table 2. The table is limited to multi-stage MMIC amplifiers (no single-stage test circuits) operating above 26.5 GHz. Under the "Test Conditions" column, we list the operating voltage and whether the results are CW or pulsed. For pulsed measurements, we list the pulsed conditions (pulse width and duty), if known.

While the table contains several entries at the upper end of Ka-band, most of the reported results are at or near 30 GHz. The data are listed chronologically starting in 2012. As expected, the power and efficiency have generally increased over time. With the exception of one foundry, which uses GaN on Si, all the reported results employ GaN on SiC substrate, either 100 µm or 50 µm thick. Clearly, the work reported in this paper represents the highest combination of power and efficiency for CW operation.

V. Ka-Band SSPA

Based on the performance of D2, we designed and fabricated a 4-way combiner-SSPA for the 31-34 GHz band. The combiner circuit, shown in Fig. 8, was realized with binary, 2-tier waveguide H-plane junctions. The back-to-back measured loss (at 34 GHz) of the divider-combiner pair was 0.4 dB or 0.2 dB for each half, including the loss of the integrated WG-to-microstrip transitions. The RF input/output ports are WR-22 waveguide. The size and weight of this SSPA are 3.45 x 2.34 x 1.25 inch^3 (87.6x59.4x31.8 mm^3) and 2.2 lbs. (1 Kg) respectively.

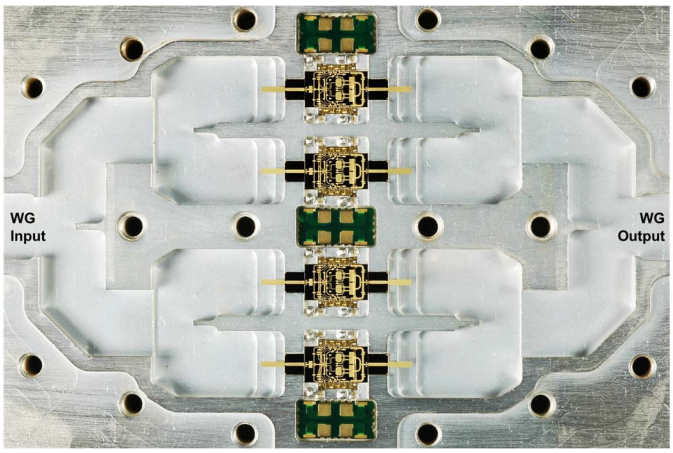

Fig. 8. Ka-band SSPA with top half removed. Size: 3.45 x 2.34 x 1.25 in^3

The SSPA performance, at a reduced bias of 24 V and an input drive level of 20 dBm, is summarized in Fig. 9. It produced an output power of greater than 20 W (24W peak) with an associated PAE of greater than 30% over the full 31 to 34 GHz band. The output power is flat at 43.5 dBm ±0.4 dB over this band.

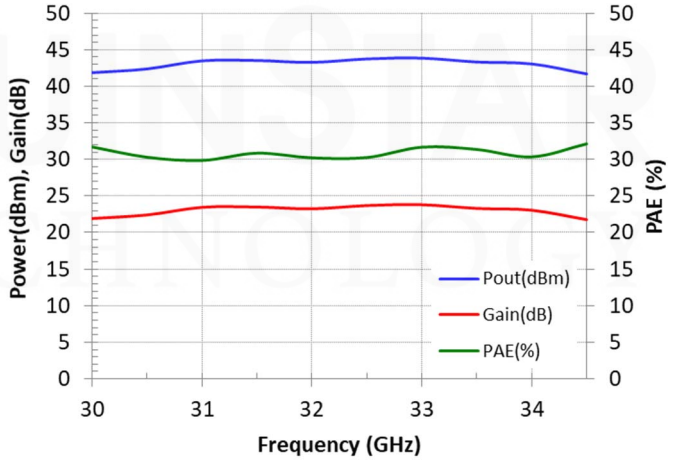

Fig. 9. Power, gain and efficiency of SSPA with Vd=24 V and Pin=20 dBm

Biased for max power at 28 V, this unit produced a P_{1dB} of 44.5 dBm and a P_{SAT} of 45.1 dBm (32.4 W) at 32.5 GHz as shown in Fig. 10. As opposed to many GaN amplifiers, the compression characteristic is very abrupt with the P_{1dB} and the P_{SAT} points separated by only 0.6 dB. Also, note that the maximum efficiency, 31%, occurs at or before P_{1dB}, not at P_{SAT}. This characteristic is particularly useful for a linear amplifier, allowing the SSPA to operate at higher power levels and better efficiencies without introducing distortion.

Table 2. Ka-Band MMIC Benchmarks

References	Freq (GHz)	Power (W)	PAE (%)	Power Gain (dB)	Test Conditions V, CW/Pulsed	No. Stages	Die Area (mm^2)
[1]	28.5	8.7	26	17.4	20V, CW	3	2.55x3.80
[2]	29	4.7	28	9.6	17V, CW	2	3x3
[3]	30	11	30	18	20V, CW	3	3.24x3.60
[4]	30	21	16	6	28V, 10µS, 10%	2	4.0x5.5
[5]	27	40	36	18.2	28V, pulsed	2	13.5
[6]	30	8.1	30	14	15V, CW	3	17.5
[7]	31	18	17	7	28V, pulsed	2	4.0x5.5
[8]	36	10	34	22	20V, 10µS, 10%	3	3.56x2.78
[9]	30	5.6	33	22.5	12V, CW	3	4.5x3.5
[10]	36	5.6	41	20	24V, 3µS, 0.3%	3	2.62x1.62
[11]	26.5	21.7	19.8	8	24V, CW	2	3.8x6.2
[12]	31	11.2	35	23	13V, pulsed	3	4.5x3.5
[13]	40	14	30	17.5	12V, 9 µS, 1%	3	3.6x2.8
[14]	28	37	27.6	24	28V, 5mS, 10%	3	17.6
This work, D1	**29.5**	**8**	**42**	**15**	**28V, CW**	**3**	**5.4x3**
This work, D2	**31.5**	**10**	**36**	**25**	**28V, CW**	**3**	**5.4x3.1**

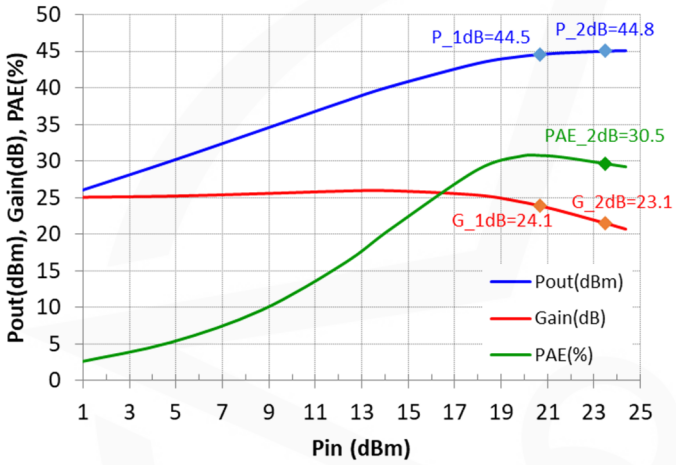

Fig. 10. SSPA output power, gain and efficiency at 32.5 GHz and 28 V.

VI. Conclusion

This work has established new power and efficiency benchmarks for MMICs operating at Ka-band frequencies. Utilizing harmonic tuning (2nd and 3rd), we have successfully demonstrated GaN MMICs producing power levels up to 10 W and efficiencies of over 40% with associated output power levels of 8 W. In contradistinction to many of the other reported results, these are CW, not pulsed, results. Further, a fully packaged (waveguide input and output) SSPA has been successfully demonstrated over the 31 to 34 GHz band, with a peak output power of 32 W and an associated PAE of 30%.

VII. Acknowledgment

This work was supported by NASA under SBIR contract NNX15CP09C.

References

[1] C. Campbell, M-Y. Kao, and S. Nayak, "High Efficiency Ka-band Power Amplifier MMICs Fabricated with a 0.15µm GaN on SiC HEMT Process," *2012 IEEE MTT IMS*, June 2012.

[2] J. Chéron, M. Campovecchio R. Quéré, D. Schwantuschke, R. Quay and O. Ambacher, "High-Efficiency Power Amplifier MMICs in 100 nm GaN Technology at Ka-Band frequencies," *2013 EuMICC*, Oct. 2013.

[3] C. Campbell, Y. Liu, M-Y. Kao, and S. Nayak, "High Efficiency Ka-Band Gallium Nitride Power Amplifier MMICs," *2013 IEEE COMCAS,* Oct. 2013.

[4] C. Ng, K. Takagi, T. Senju, K. Matsushita, H. Sakurai, K. Onodera, S. Nakanishi, K. Kuroda, T. SoejimaJ. "A 20-Watt Ka-Band GaN High Power Amplifier MMIC," *2014 EuMICC, Oct. 2014.*

[5] S. Din, M. Wojtowicz, and M. Siddiqui, "High power and high efficiency Ka band power amplifier," *2015 IEEE MTT IMS*, May 2015.

[6] J. Chéron, M. Campovecchio, R. Quéré, D. Schwantuschke, R. Quay, and O. Ambacher, " High-gain Over 30% PAE Power Amplifier MMICs in 100 nm GaN Technology at Ka-Band Frequencies," *2015 EuMICC,* Oct. 2015.

[7] K. Takagi, C. Ng, H. Sakurai, K. Matsushita, "GaN MMIC for Ka-Band with 18W," *2015 CSICS*, Oct. 2015.

[8] S. Chen, S. Nayak, C. Campbell, and E. Reese, "High Efficiency 5W/10W 32 - 38GHz Power Amplifier MMICs Utilizing Advanced 0.15µm GaN HEMT Technology," 20*16 IEEE* CSICS.

[9] R. Leblanc, N. Ibeas, A. Gasmi, F. Auvray, J. Poulain, F. Lecourt, G. Dagher, and P. Frijlink, "6W Ka band power amplifier and 1.2dB NF X-band amplifier using a 100nm GaN/Si process," *2016 IEEE CSICS.*

[10] P. Blount, S. Huettner, and B. Cannon, "A High Efficiency, Ka-Band Pulsed Gallium Nitride Power Amplifier for Radar Applications," *2016 IEEE CSICS.*

[11] Y. Yamaguchi, J. Kamioka, M. Hangai, S. Shinjo, and K. Yamanaka, "A CW 20W Ka-band GaN High Power MMIC Amplifier with a Gate Pitch Designed by Using One-Finger Large Signal Models," *2017 IEEE CSICS.*

[12] A. Gasmi, M. Kaamouchi, J. Poulain, B. Wroblewski, F. Lecourt, G. Dagher, P. Frijlink, and R. Leblanc, "10W Power amplifier and 3W Transmit/Receive module with 3 dB NF in Ka band using a 100nm GaN/Si process," *2017 IEEE CSICS.*

[13] J. Moron, R. Leblanc, F. Lecourt, and P. Frijlink, "12W, 30% PAE, 40 GHz power amplifier MMIC using a commercially available GaN/Si process," *2018 IEEE IMS*, June 2018.

[14] M. Roberg, T. Kywe, M. Irvine, O. Marrufo and S. Nayak "40W Ka-Band Single and Dual Output GaN MMIC Power Amplifiers on SiC," *2018 IEEE BCICT Sym.*, Oct. 2018.